Finally, the Applicants have amended the Abstract so as to address the objection thereto set forth in paragraph 1 of the Office Action.

Applicants also note with appreciation the indication of allowable subject matter being recited by claims 4-8 and 10.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art.

II. The Rejection Of The Claims Under 35 U.S.C. § 112, Second Paragraph

Claims 1-10 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. In addition, claims 1-10 were objected to for the reasons set forth in paragraph 2 of the Office Action. In response, Applicants have amended claims 1-10 so as to address each of the points raised with regard to both the objections and rejections of claims 1-10 under 35 U.S.C. § 112, second paragraph. Applicants wish to thank the Examiner for her assistance in correcting the claims.

Accordingly, as each of the issues noted in the pending rejection have been addressed by the foregoing amendment of the claims. It is respectfully submitted that both the objections to claims 1-10 and the rejection of claims 1-10 under 35 U.S.C. § 112, second paragraph, have been overcome.

III. The Rejection Of Claims 1-3 And 9 Under 35 U.S.C. § 103

Claims 1-3 and 9 were rejected under 35 U.S.C. § 103 as being unpatentable over USP No. 5,471,409 to Tani. Applicants respectfully submit that, as amended, claims 1 and 9 are clearly patentable over Tani for at least the following reasons.

As recited by both claims 1 and 9, the present invention relates to a verification method (and a circuit for performing the same) wherein a step of verifying that the circuit elements of the semiconductor circuit being verified utilizing the loaded condition information is performed **concurrently** with the step of simulating operation of the semiconductor circuit being verified. Thus, in accordance with the present invention, during the simulating operation step of the semiconductor circuit being verified, it is concurrently determined whether or not the circuit elements satisfy voltage and/or current specifications every time voltage and/or current computation results are stored in memory (i.e., the verification step). For further details of the present invention, see, e.g., page 14, line 15 to page 15, line 4 of the specification.

As a result of the foregoing process, the method of the present invention enables high-speed operation of the verification step, which determines whether or not the circuit elements being verified satisfy the loaded condition requirements. Moreover, the present invention eliminates the requirement of having sufficient memory (e.g., a hard disk drive) for storing the results/data of the entire operation simulation, which is required when performing the verifying step subsequent to the simulation operation step. Thus, the present invention allows for the foregoing testing utilizing a relatively inexpensive computation system.

Turning to the cited prior art, it is clear that Tani fails to disclose or suggest a method or system in which the simulation operation step and the condition verifying step are performed concurrently as taught by the present invention. Indeed, in contrast to the present invention, it appears Tani is practicing the practicing the prior art disclosed in the background section of the Applicants' specification, wherein the circuit simulation is performed first and all results are stored in a large-capacity memory device, such as a hard disk, which operates at a low speed, and thereafter (i.e., once the circuit simulation is complete) the loaded condition verification task is performed using the data stored in the large-capacity memory device. Thus, at a minimum, Tani fails to disclose or suggest the step of verifying that the circuit elements satisfy the loaded condition information **concurrently** with the step of simulating operation of the semiconductor circuit.

Accordingly, as each and every claim limitation must be disclosed or suggested by the prior art reference in order to establish a *prima facie* case of obviousness (*see*, M.P.E.P. § 2143.03), and Tani fails to do so for at least the foregoing reasons, it is respectfully submitted that claims 1 and 9, as amended, are patentable over Tani.

IV. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as all pending independent claims are patentable for the reasons set forth

above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

V. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 5/5/03

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

The Abstract beginning at page 45, line 2, has been amended as follows:

In [a] the circuit operation verifying method, initialization includes inputting circuit diagram data (a net lest), specification information on respective circuit elements, and input data representing waveforms with time of voltages or currents used for operation simulation, and [expanding] storing the circuit diagram data to memory. Operation of a semiconductor circuit to be verified is simulated using the circuit diagram data and the input data, and momentary voltage/current values at input terminals and the like of the circuit elements are stored in the memory. During the operation simulation, whether or not the circuit elements satisfy their voltage/current specifications and time specifications are concurrently verified based on the voltage/current values stored in the memory.

IN THE CLAIMS:

Claims 1-10 have been amended as follows:

1. (Amended) A circuit operation verifying method for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the method comprising the steps of:

loading condition information as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit to be verified, and input patterns of voltages and currents used for circuit operation simulation with respect to time;

simulating operation of the semiconductor circuit to be verified while computing voltage values or current values with respect to time [at] of the circuit elements of the semiconductor circuit [to be] being verified based on the loaded circuit diagram data and input patterns and storing the computed values in a memory; and

verifying that the circuit elements of the semiconductor circuit [to be] being verified satisfy the loaded condition information using the voltage values or the current values [at] of the circuit elements stored in the memory, said verification being performed concurrently with said simulating operation.

2. (Amended) The [device] method of Claim 1, wherein the condition information includes electrical specifications representing current density values and heat generation amounts of the circuit elements, the circuit diagram data of the semiconductor circuit [to be verified] includes layout information, and

current density analysis and heat generation analysis at positions inside the semiconductor circuit [to be verified] are performed based on the current values [at] of the circuit elements and the layout information stored in the memory.

3. (Amended) The method of Claim 1, wherein the condition information includes time specifications representing the frequency of violation against the electrical specifications or the time period for which a violation state is allowable, and

whether or not the frequency of violation or the violation allowable time period of each of the circuit elements of the semiconductor circuit [to be] being verified satisfy the time specifications is [verified] determined using the voltage values or the current values

with respect to time [at] of the circuit element stored in the memory.

4. (Amended) The method of Claim 1, wherein upon termination of the operation simulation and [the] a condition verification of the semiconductor circuit [to be verified], results of the condition verification are displayed on a waveform display apparatus displaying results of the operation simulation or a design apparatus used for circuit design or layout design of the semiconductor circuit.

5. (Amended) The method of Claim 1, wherein a verification period during which [the] a condition verification is to be executed for the semiconductor circuit [to be verified] or a non-verification period during which no condition verification is to be executed is designated[,]; and

the condition verification for the semiconductor circuit [to be verified] is executed during the verification period, or the no condition verification for the semiconductor circuit [to be verified] is executed during the non-verification period.

6. (Amended) The method of Claim 1, wherein the specifications in the condition information are commonly designated for all the circuit elements of the semiconductor circuit [to be] being verified, or individually designated for the respective circuit elements.

7. (Amended) The method of Claim 6, wherein a low-precision, high-speed operation simulation is executed for the semiconductor circuit [to be verified] using the

input patterns, to prepare operation information on the circuit elements of the semiconductor circuit [to be] being verified and circuit hierarchical information on the semiconductor circuit to be verified[,];

[thereafter,] wherein a plurality of circuit portions, each having [the same] an operation pattern and [the same] a hierarchical state, in the semiconductor circuit [to be verified] are retrieved based on the operation information, the circuit hierarchical information, and the circuit diagram data[,]; and

wherein the specifications in the condition information are individually designated for only one circuit portion among the retrieved plurality of circuit portions so that [the] a condition verification is executed for only circuit-elements included in the one circuit portion.

8. (Amended) The method of Claim 1, wherein low-precision, high-speed operation simulation is executed for the semiconductor circuit [to be verified] using the input patterns, to prepare operation information on the circuit elements of the semiconductor circuit [to be] being verified and circuit hierarchical information on the semiconductor circuit [to be verified,];

[thereafter,] wherein a plurality of circuit portions having the same operation pattern and the same hierarchical state in the semiconductor circuit [to be verified] are retrieved based on the operation information, the circuit hierarchical information, and the loaded circuit diagram data[,]; and

wherein the retrieved plurality of circuit portions are united into one circuit portion, to reduce the circuit diagram data.

9. (Amended) A circuit operation verifying apparatus for verifying that each of a number of circuit elements of a semiconductor circuit in layout design satisfies specifications, the apparatus comprising:

loading means for loading condition information as electrical specifications on voltages and currents applied to the circuit elements, circuit diagram data representing connection information of the semiconductor circuit to be verified, and input patterns of voltages and currents used for circuit operation simulation with respect to time;

operation simulation means for simulating operation of the semiconductor circuit [to be] being verified while computing voltage values or current values with respect to time [at] of the circuit elements of the semiconductor circuit [to be] being verified based on the circuit diagram data and the input patterns loaded by the loading means and storing the computed voltage values or current values in a memory; and

verification means for verifying that the circuit elements of the semiconductor circuit [to be] being verified satisfy the specifications in the loaded condition information using the voltage values or the current values [at] of the circuit elements stored in the memory,

said verification means performing said verification concurrently with said operation simulation means performing said simulating operation.

10. (Amended) The apparatus of Claim 9, further comprising:

waveform display means for displaying results of the operation simulation of the semiconductor circuit [to be] being verified performed by the operation simulation

means; and

design means used for circuit design or layout design of a semiconductor circuit,

wherein the results of the condition verification of the semiconductor circuit [to be] being verified performed by the verification means are displayed on the waveform display means or the design means.